Tutorial Lab : Memory Blocks

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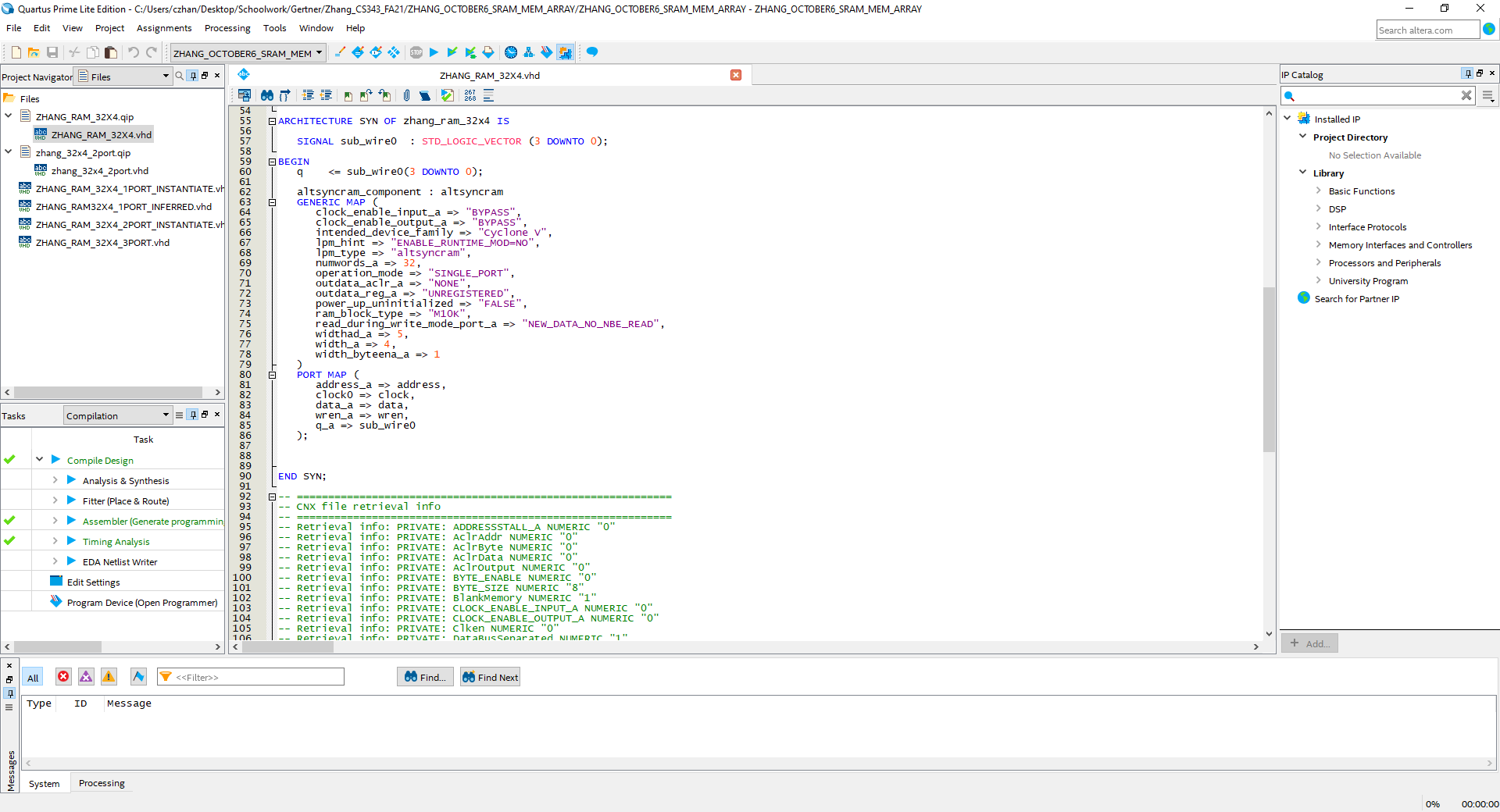
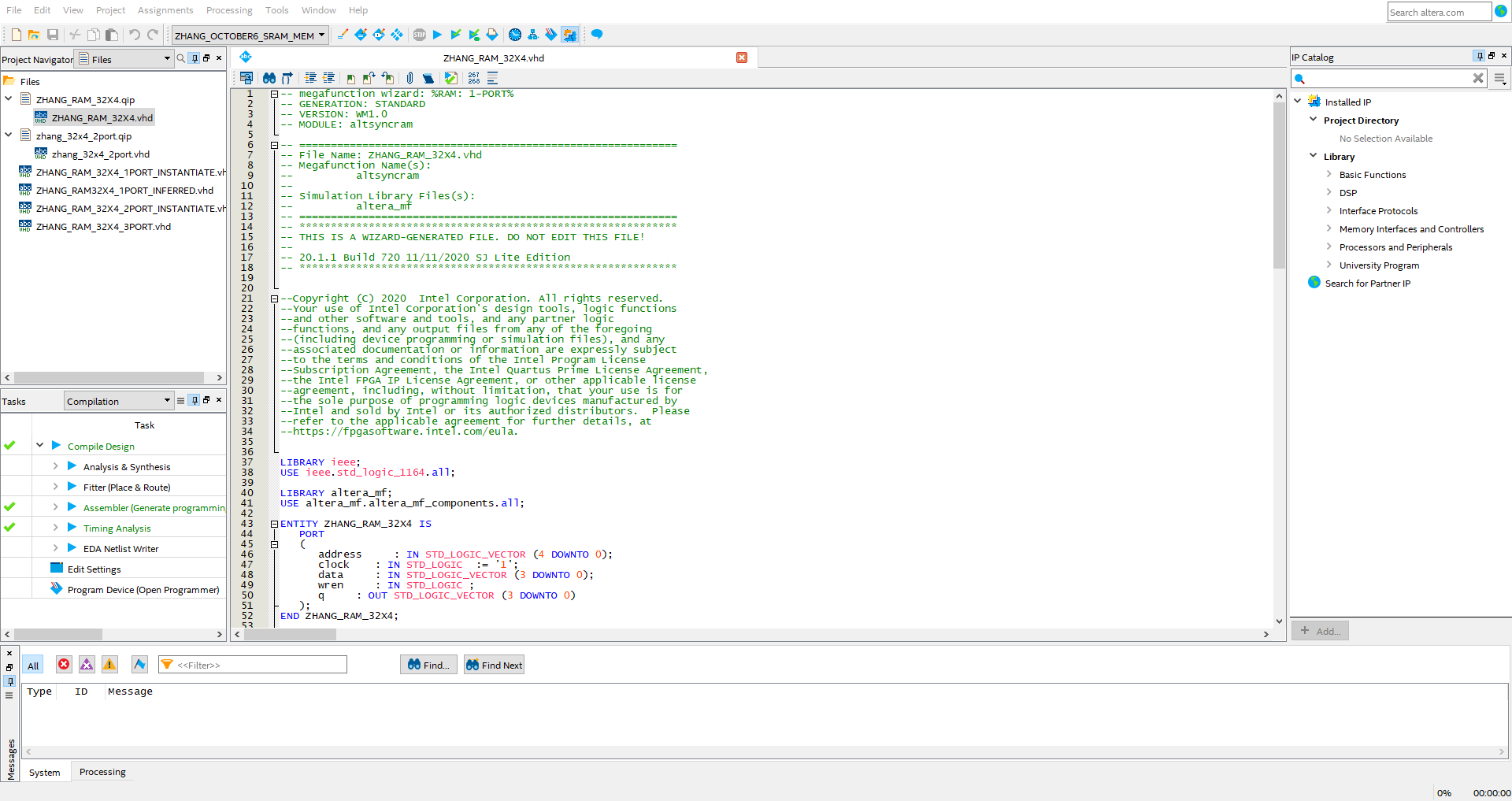
Part IV

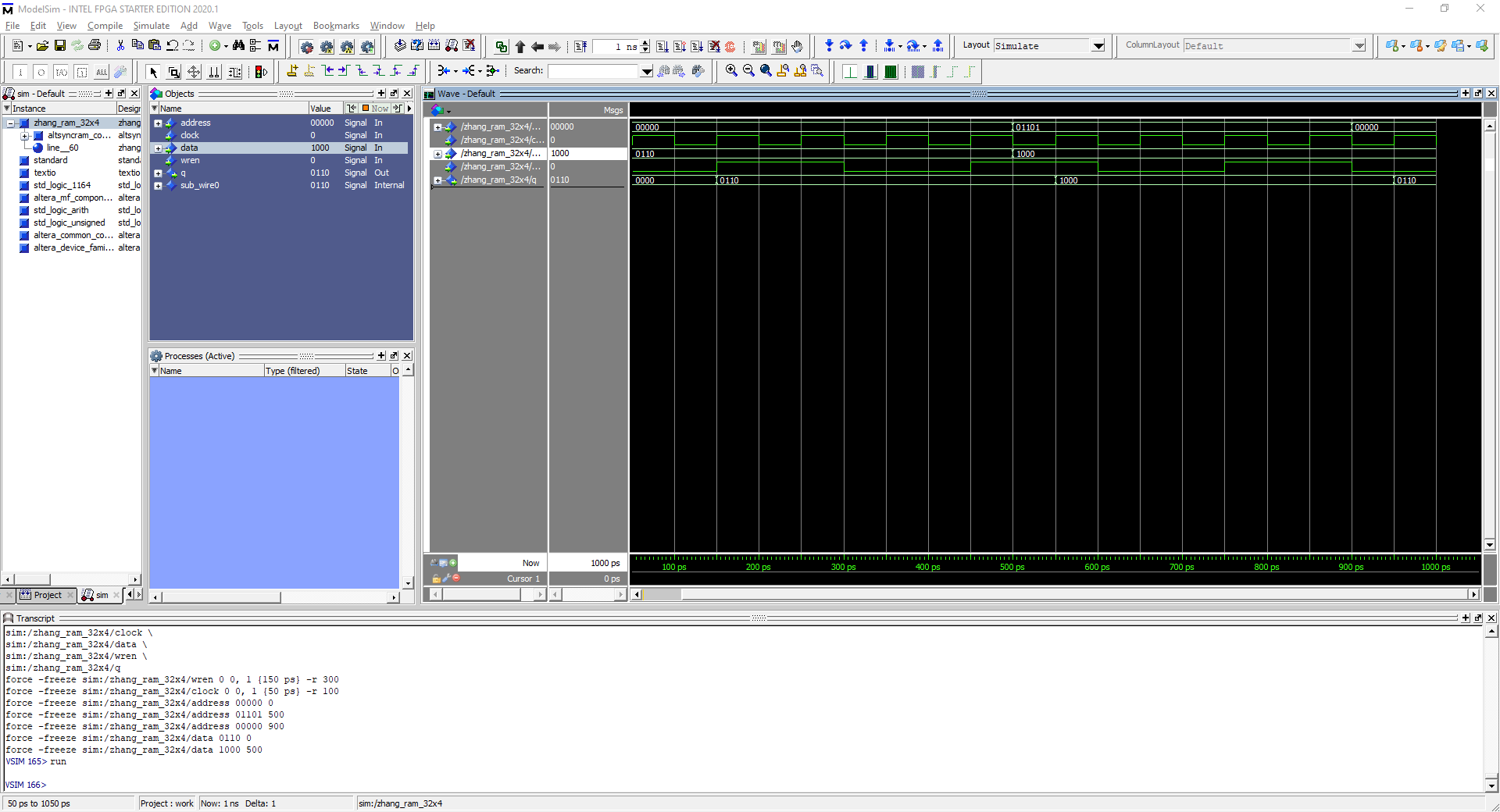
LPM generated 32x4 ram 2 port…………………………………………………………………………………………………………………10

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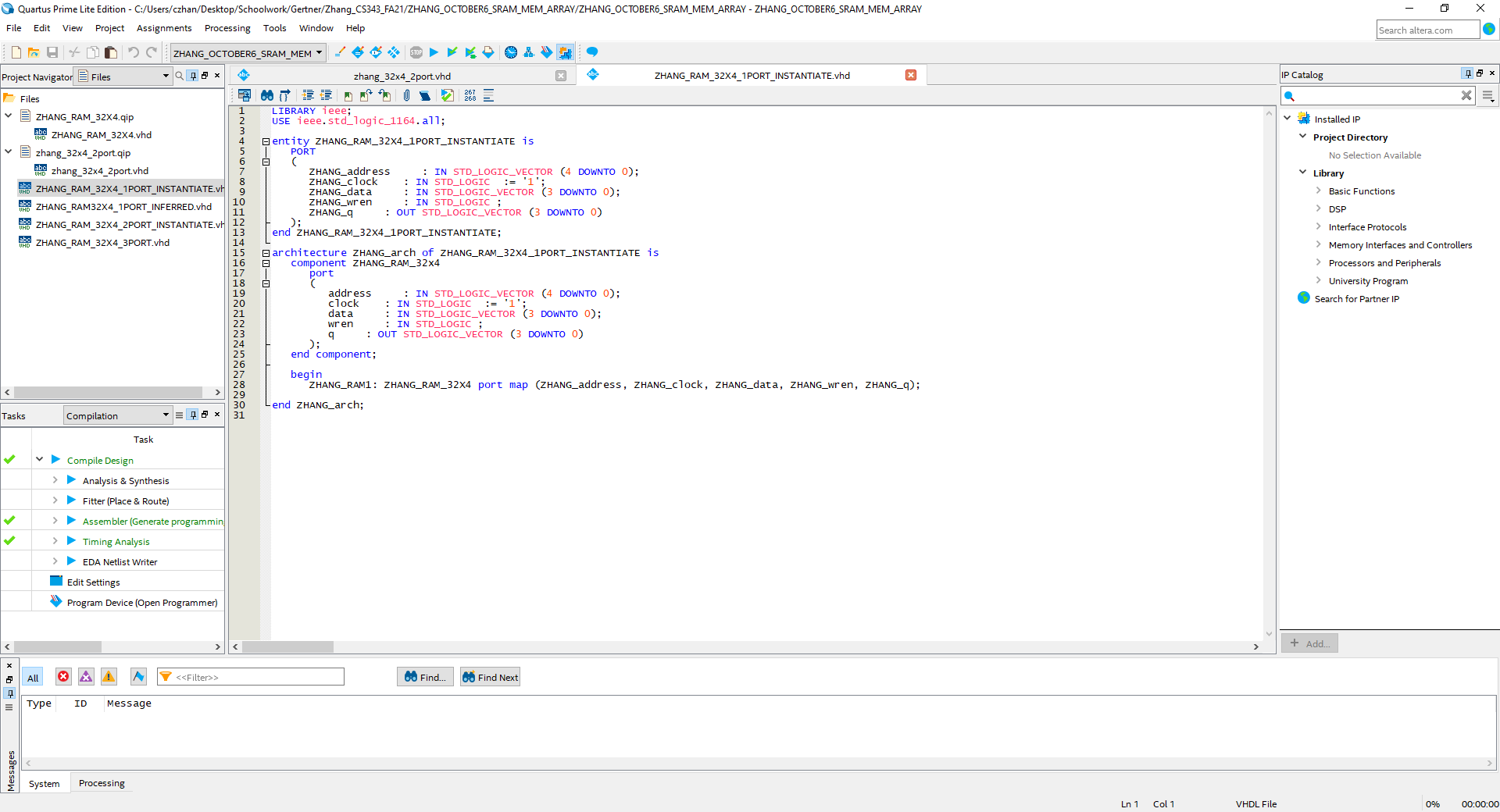
Part V

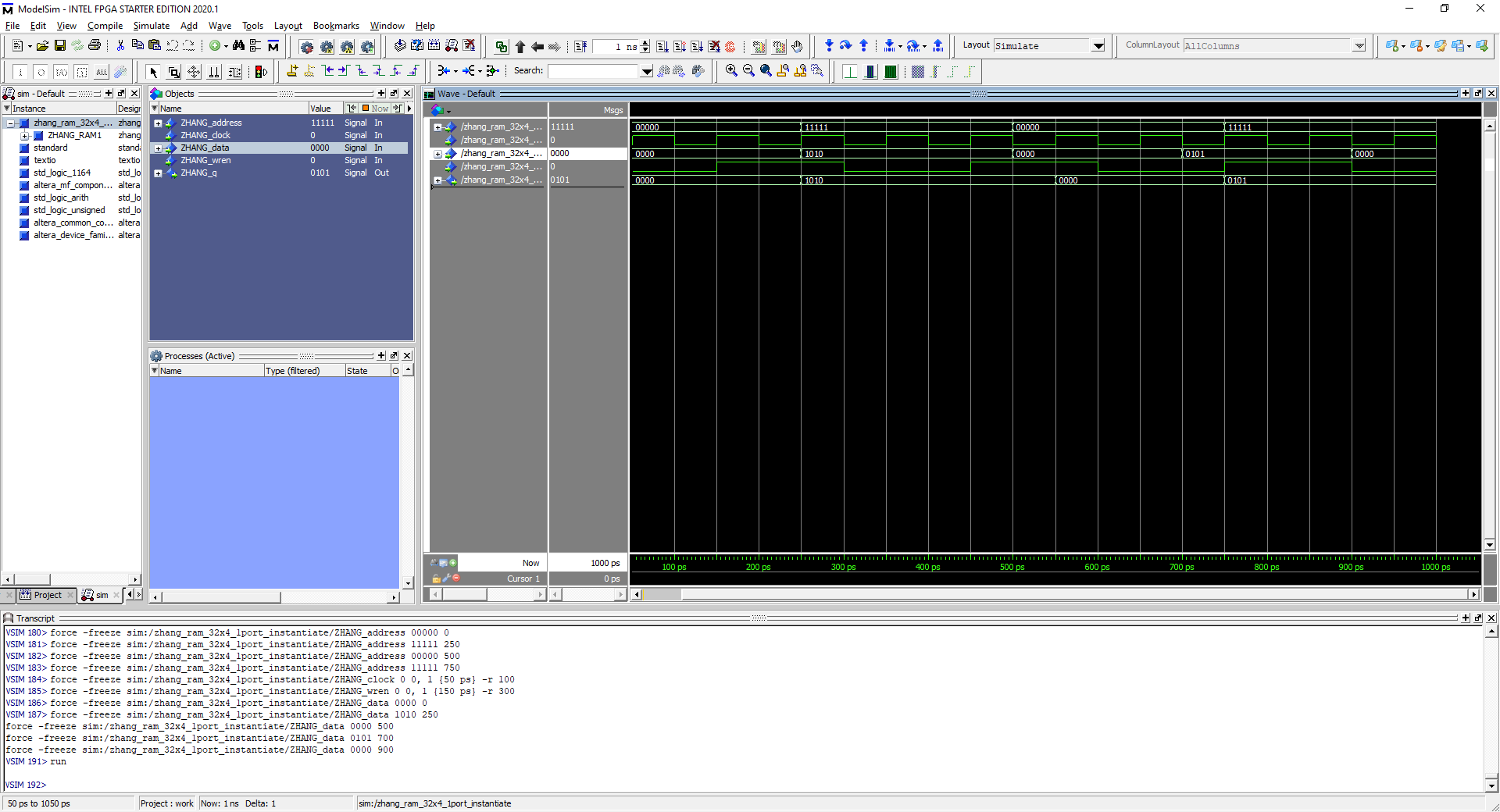
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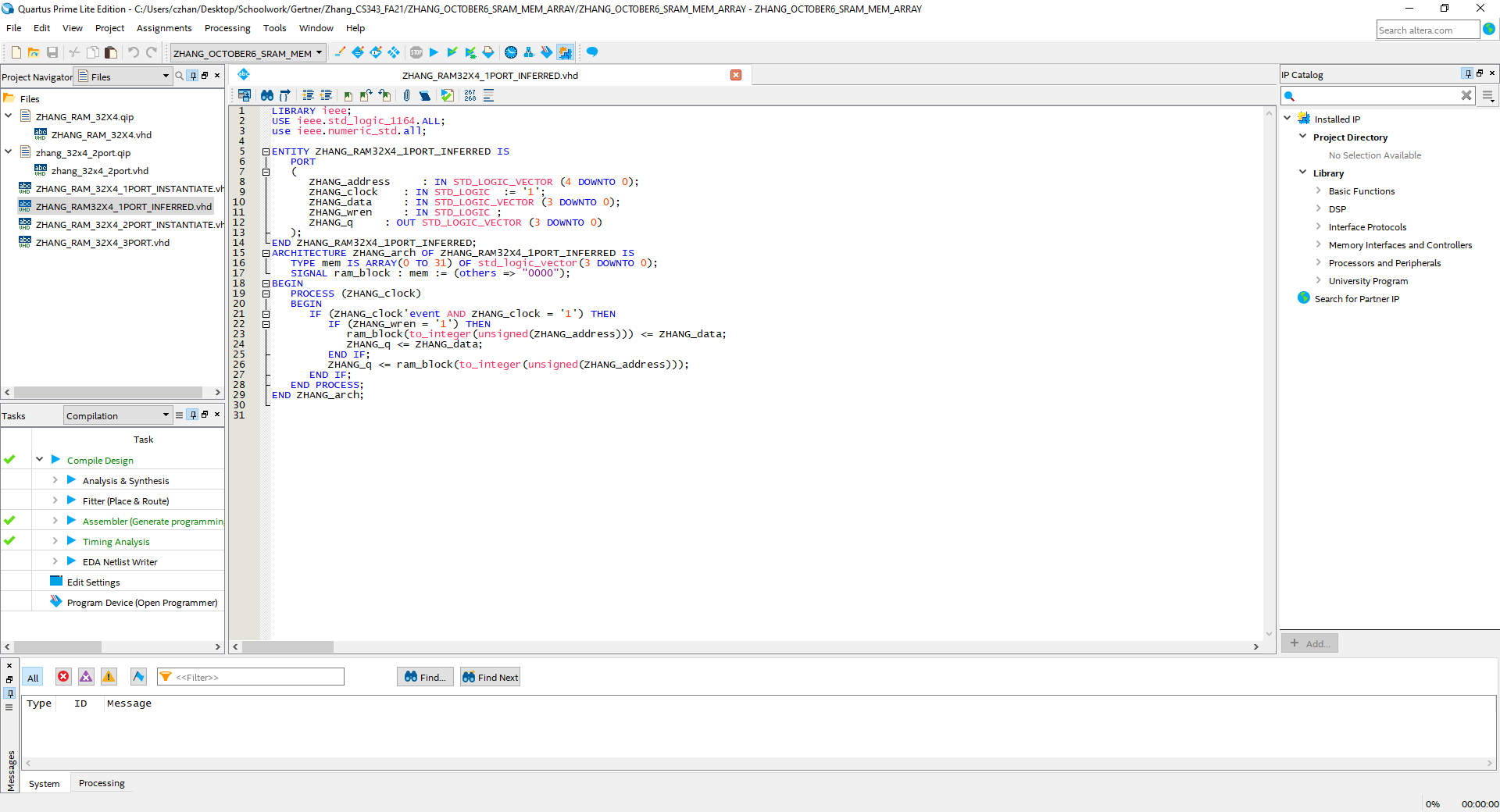


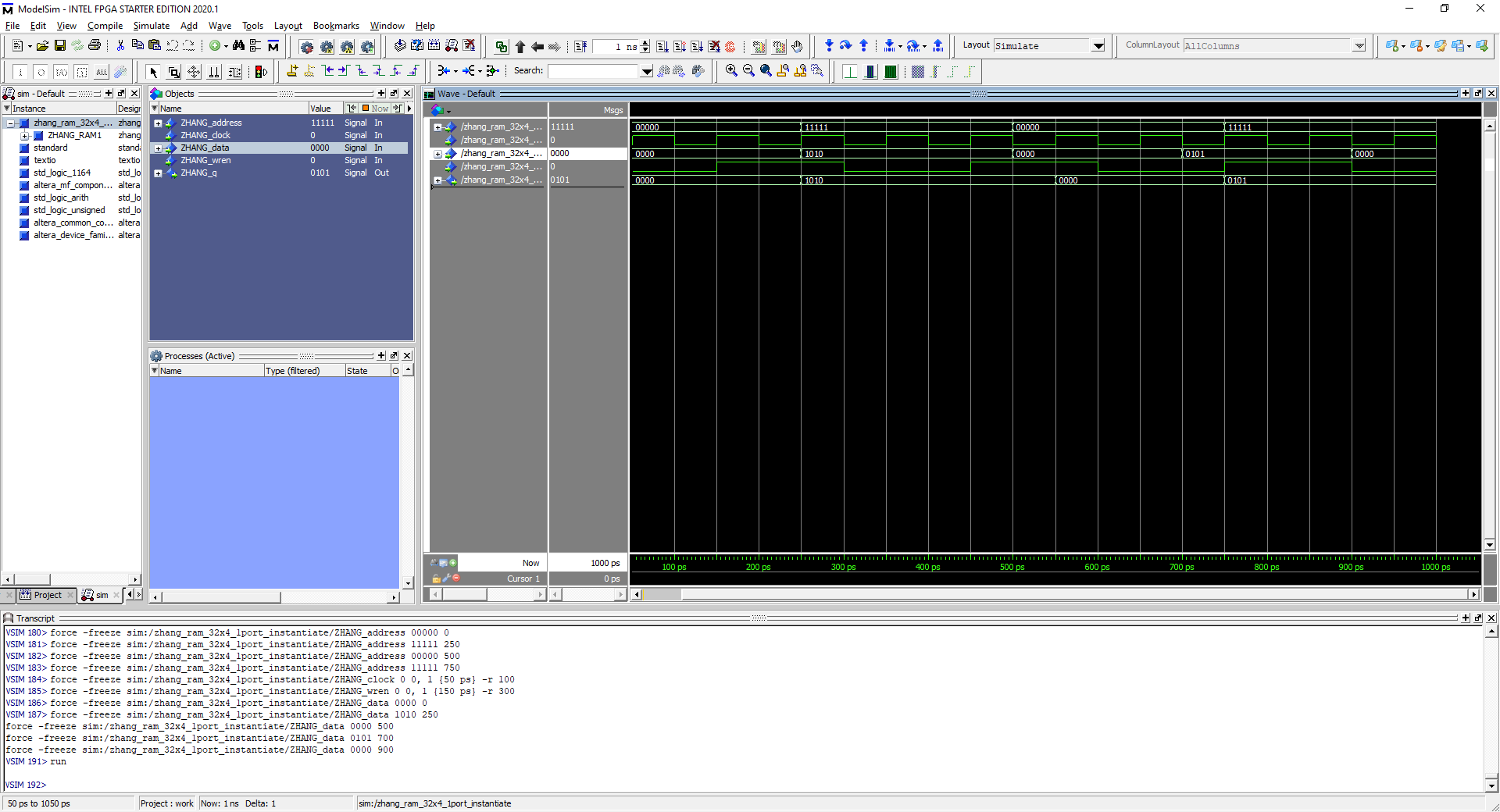
Modelsim testing outputs of the 1 port LPM generated with address of 00000 at 0ps, 01101 at 500ps, 00000 at 900ps.



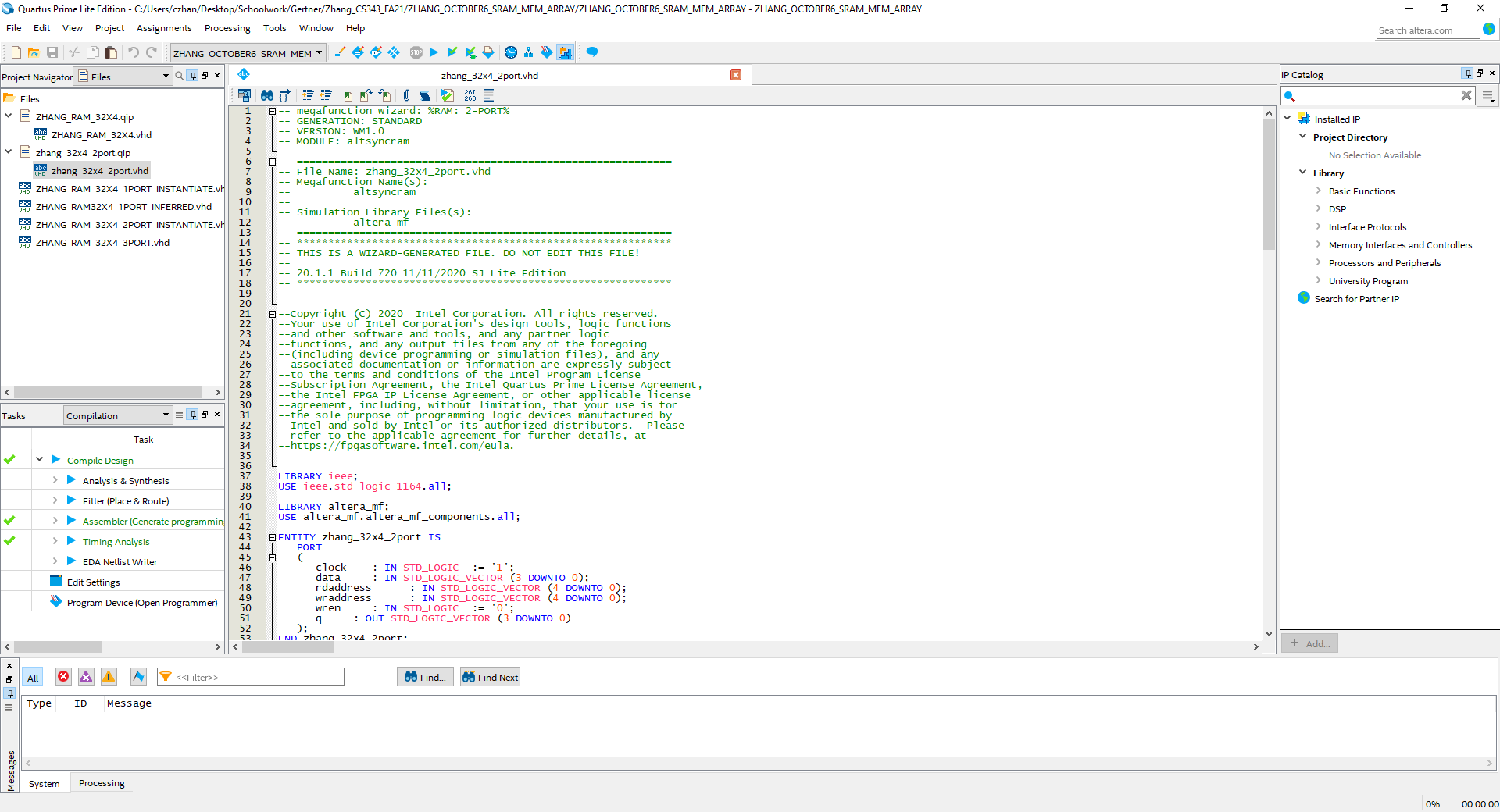


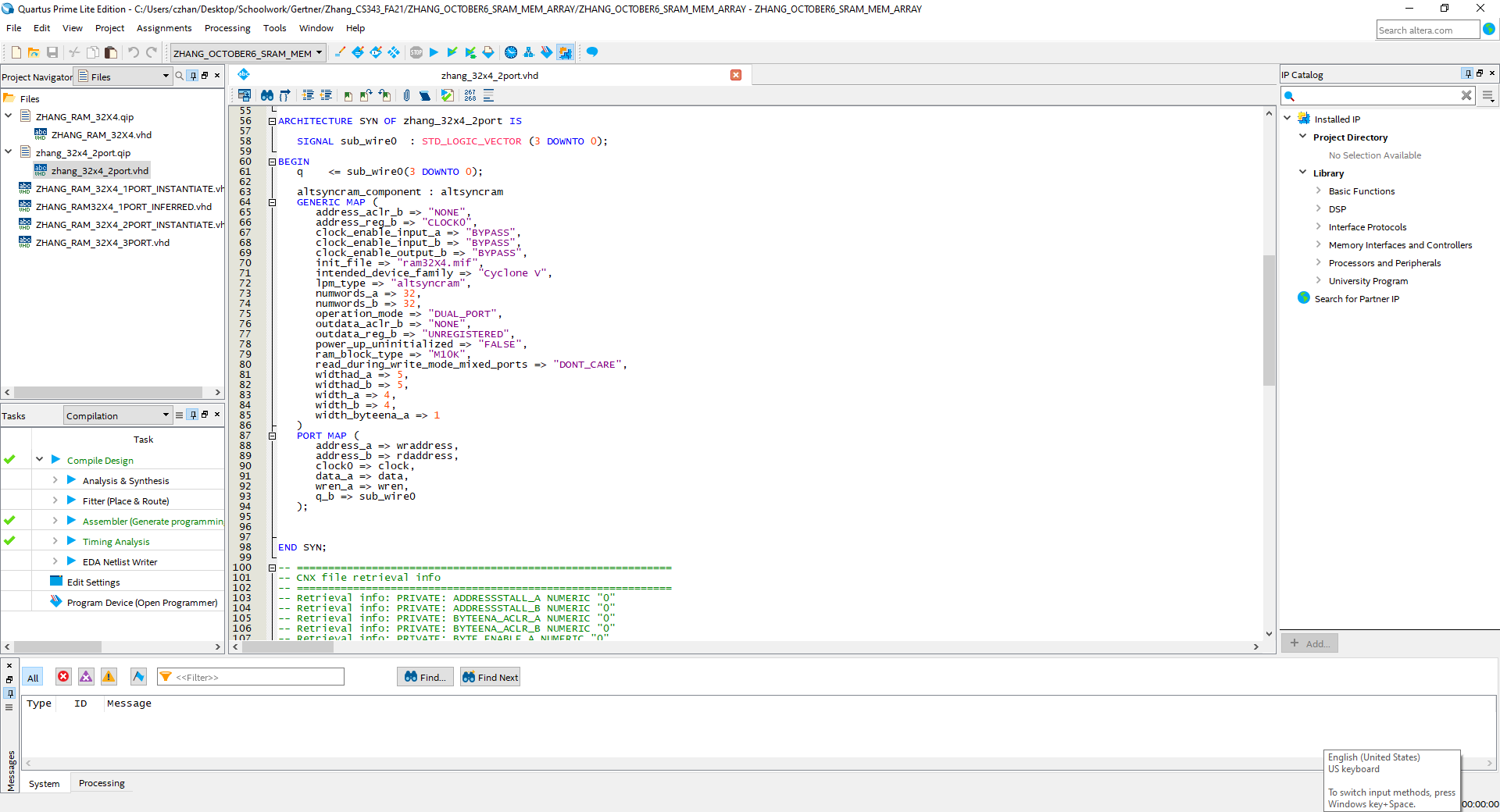
Testing with the same inputs as before and comparing, no differences and no errors.

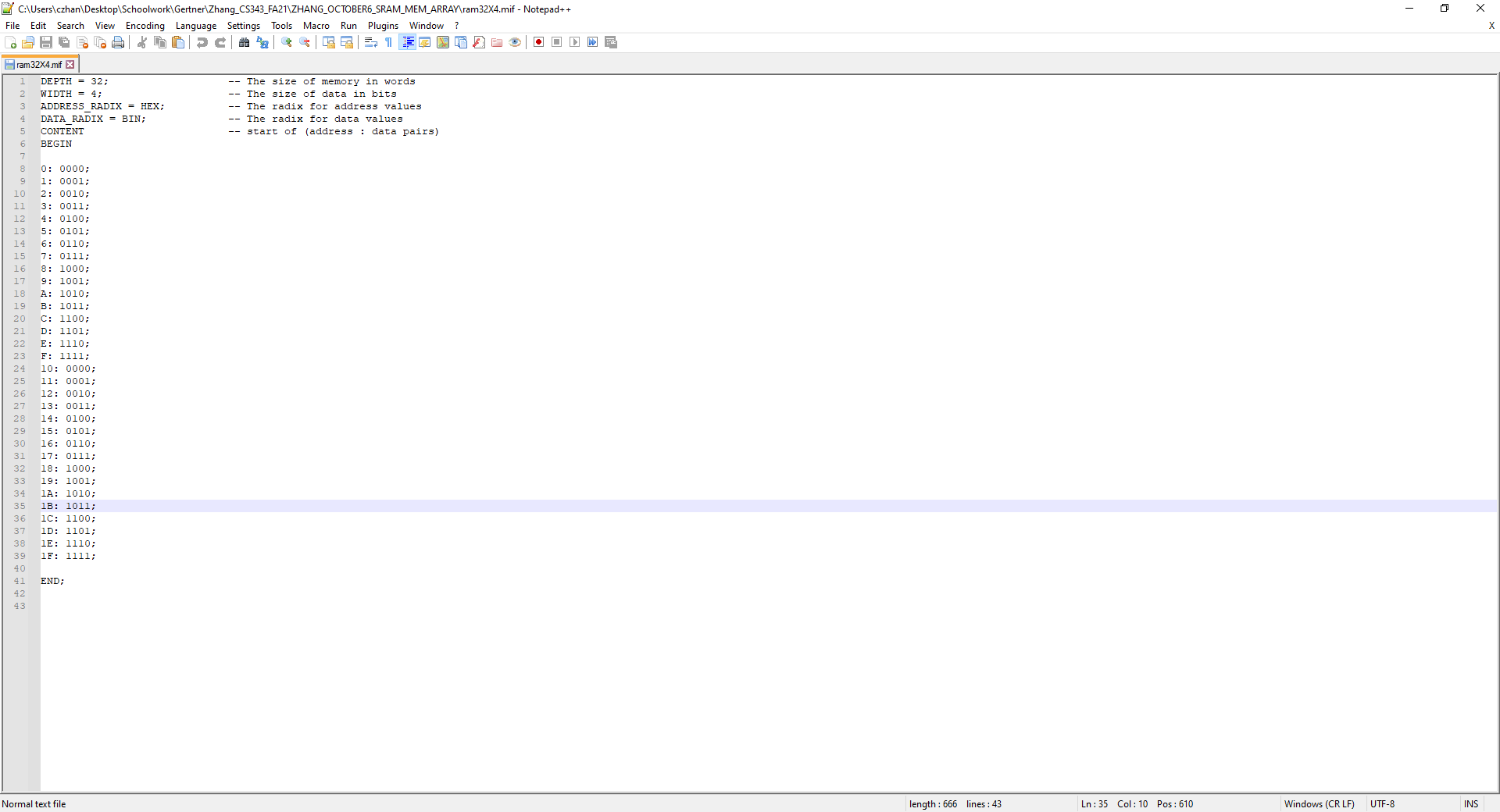


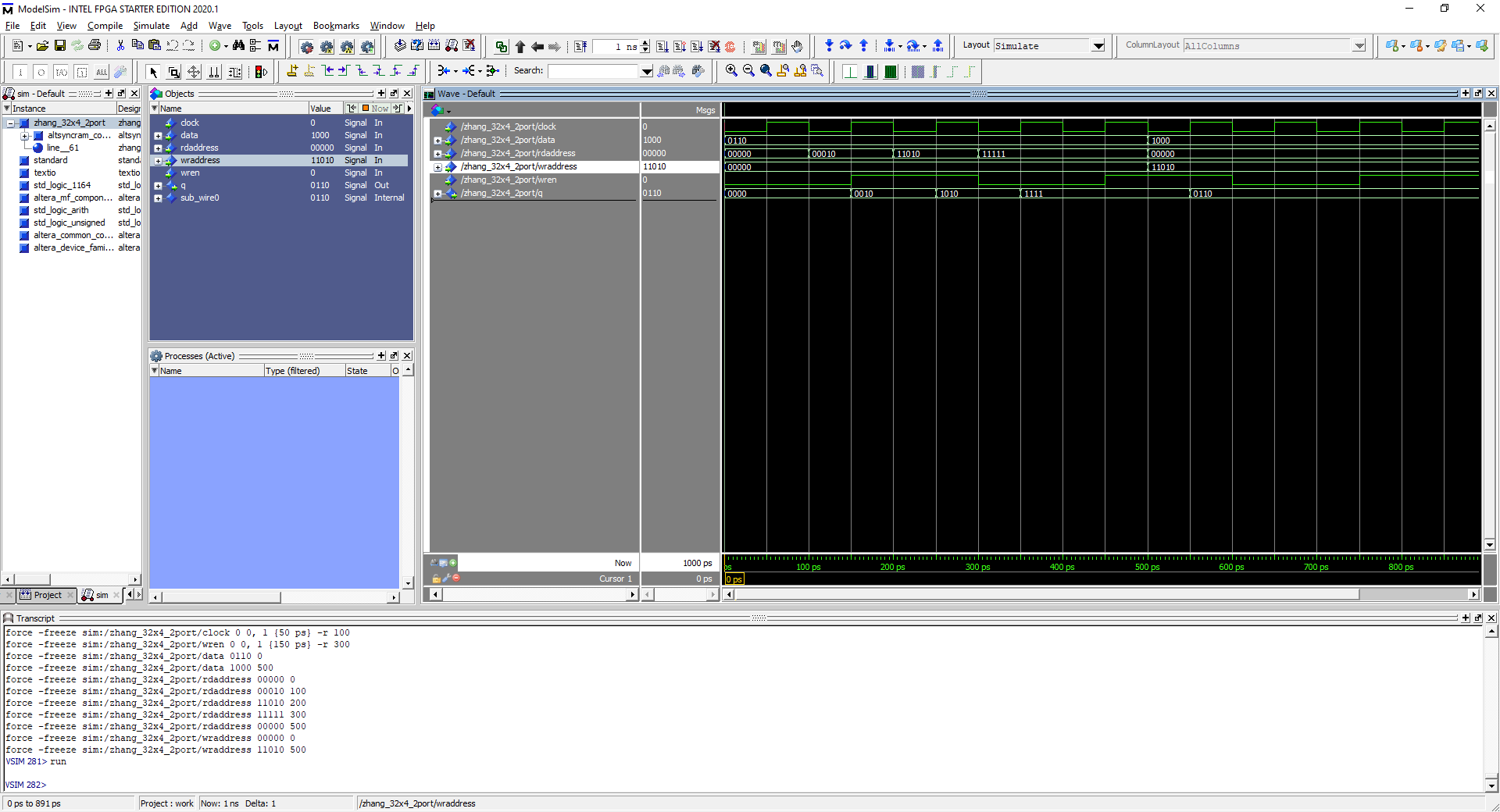


Testing with the same input as before when testing 1 port RAMS, no difference.

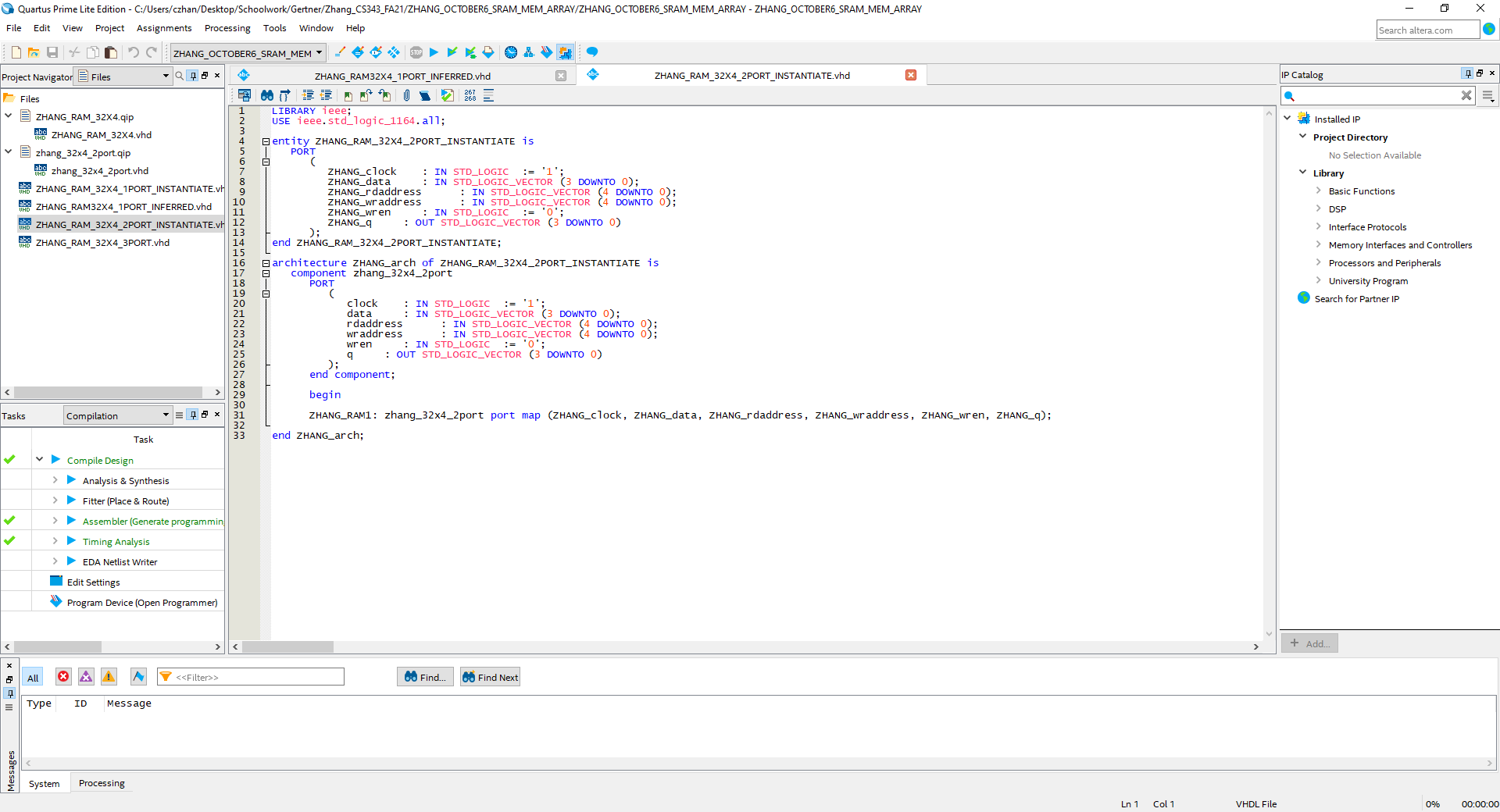


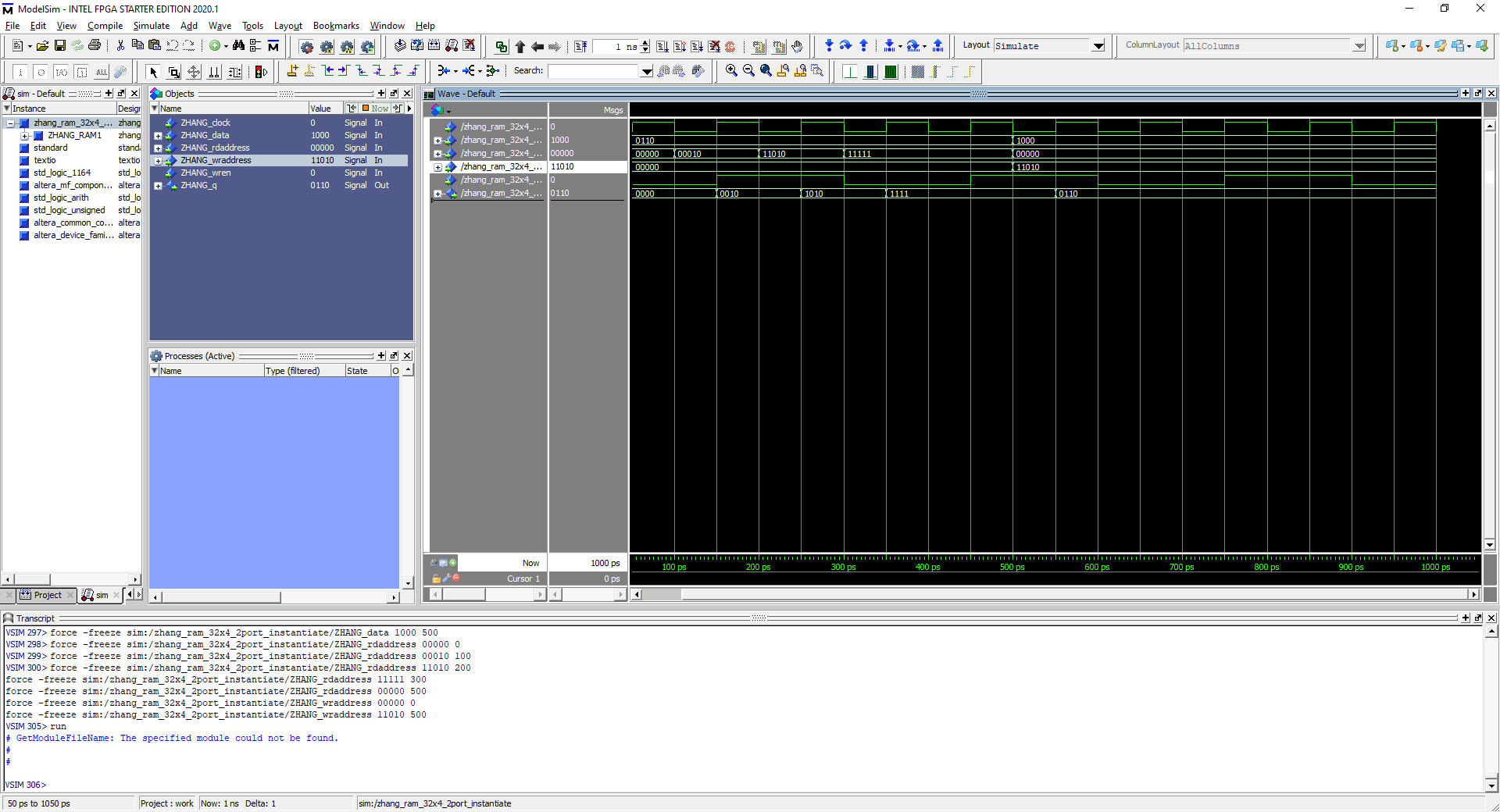




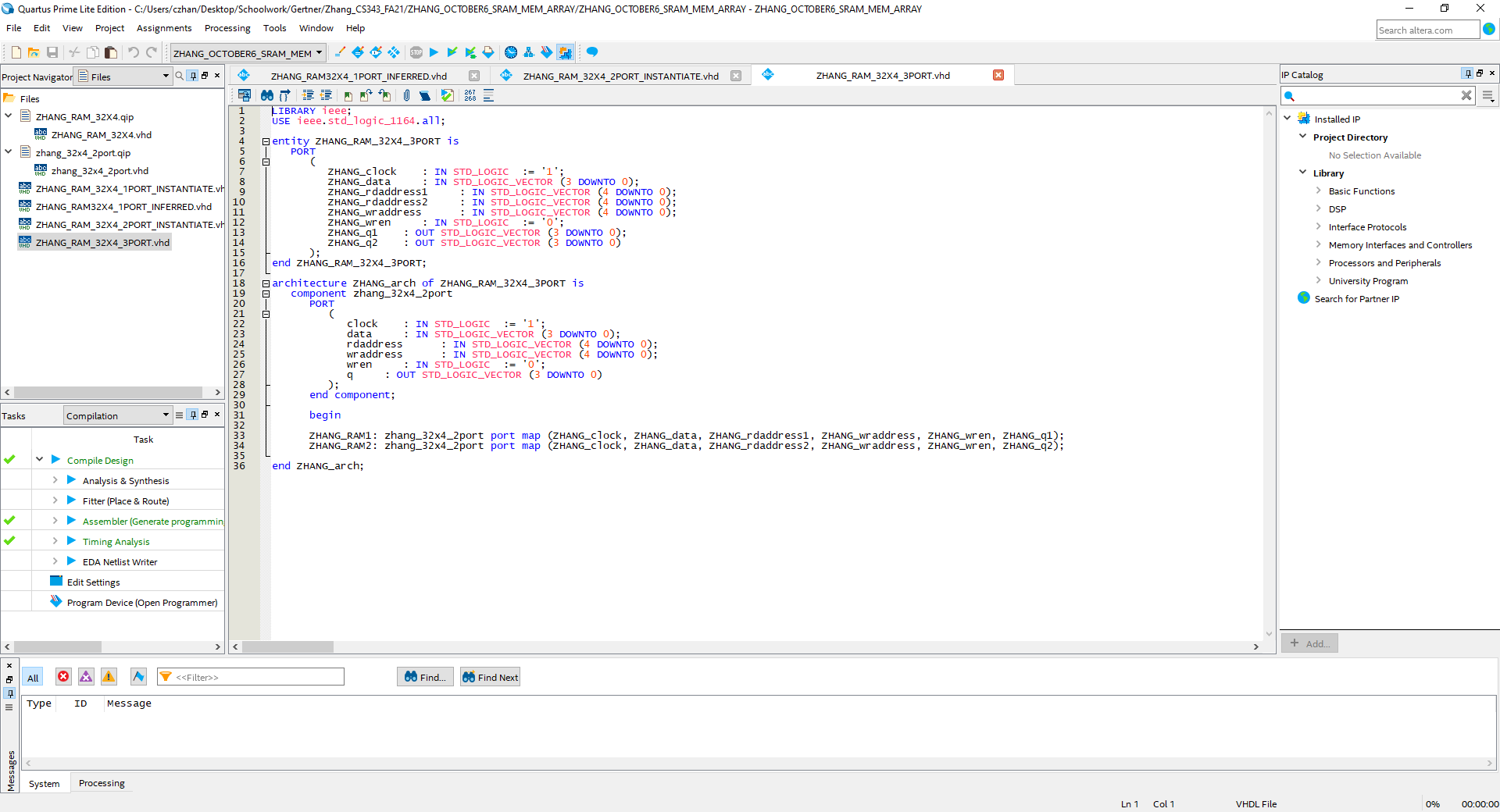


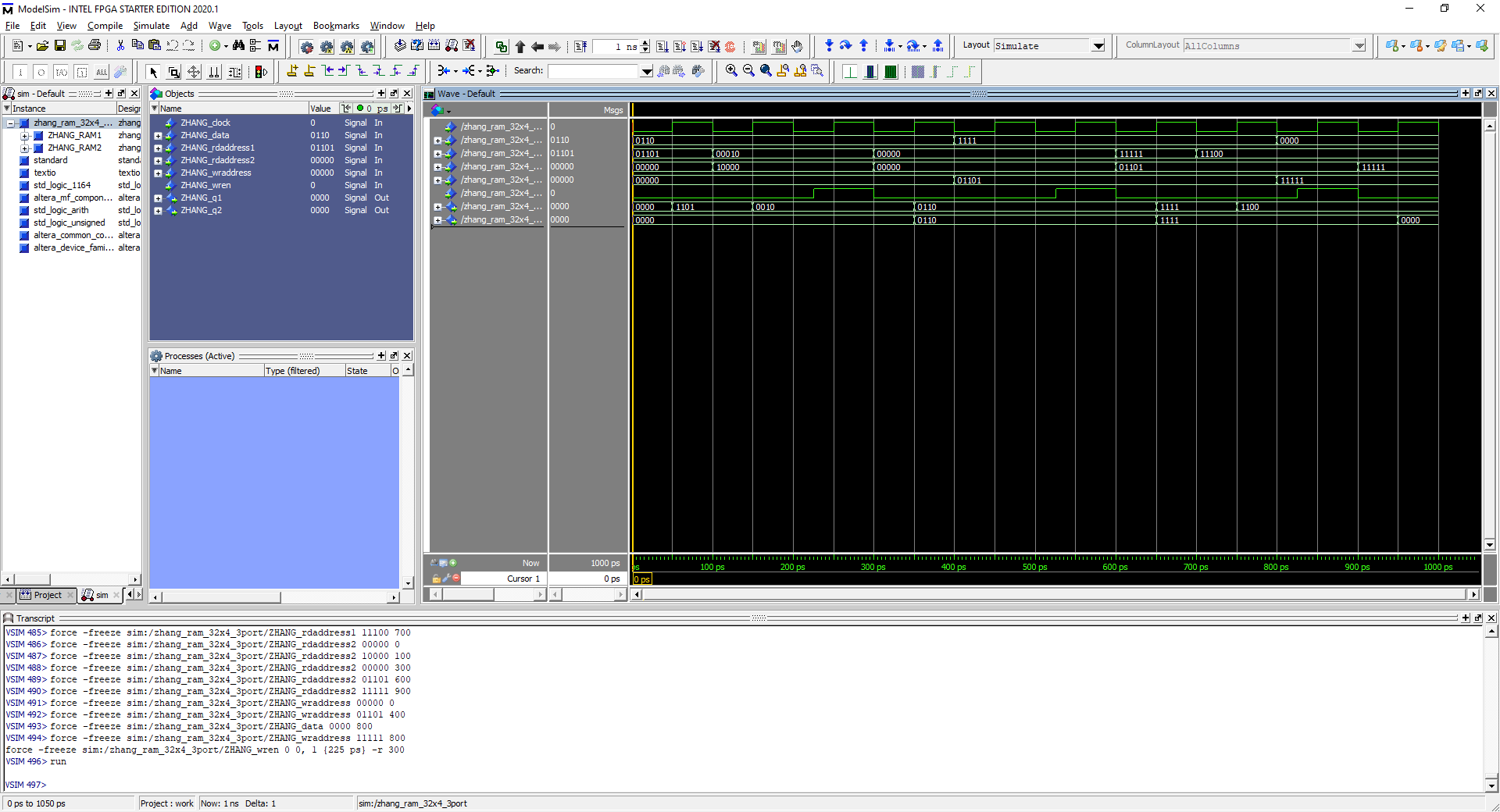
2 port LPM generated file and testing with a clock on block wren and clock. No errors





Testing using instantiated 2 port Ram with the same test inputs with no errors and no differences.





Testing inputs with a 3 port ram which uses 2, 2 port rams. Above showcases two address inputs that needs to be read and one write.